

REMARKS

This is in response to the Office Action of December 3, 2003. Claims 1-23 were rejected. Claims 1, 3, 5, 7, 8, 10, 11, 16, 18, and 20 were amended. Claims 1-23 are pending.

The Examiner rejected claims 3, 5, 16, and 18 under 35 U.S.C. §112. In regards to claims 3 and 16, Applicant has clarified the meaning of "outstanding." Outstanding has a common meaning of "uncollected." Outstanding trace data is thus trace data that has not been collected for tracing. As described in Applicant's specification in paragraphs [1038] to [1041] load data may not be immediately available such that the transmission of load data is deferred until the load data is returned from memory. In regards to claims 5 and 18, a load address may be traced out before load data, which may occur, for example, the load data is delayed due to a cache miss, as described in paragraphs [1034] to [1041]. Applicant has amended claims 5 and 18 to clarify that the load address may be transferred before the associated load data.

The Examiner has rejected all of the pending claims under 35 U.S.C. 103(a) on the basis of Miura et al (U.S. Pat. No. 5,625,785) and Miyake (U.S. Pat. No. 5,404,47) and other references, depending upon the claims at issue. The Examiner rejected claims 1, 2, 7, 8, 9, and 10 under 35 U.S.C. 103(a) over Miura et al. (U.S. Pat. No. 5,625,785) in view of Miyake (U.S. Pat No. 5,404,470). Claim 3 was rejected under 35 U.S.C. 103(a) over Miura in view of Miyake and further in view of Hicks (U.S. Pat. No. 5,150,470). Claims 4-6 and 17-19 were rejected under 35 U.S.C. 103(a) over Miura in view of Miyake and further in view of Levine (U.S. Pat. No. 5,878,208). Claims 11-15 and 20-23 were rejected under 35 U.S.C. 103(a) over Miura in view of Miyake and further in view of Swaine et al. (U.S. Publication No. 2002/0127965). Claim 16 was rejected under 35 U.S.C. 103(a) over Miura in view of Miyake and further in view of Swaine and Hicks. Claims 17-19 were rejected under 35 U.S.C. 103(a) over Miura in view of Miyake in view of Swaine and further in view of Levine (U.S. Pat. No. 5,878,208). Applicant respectfully traverses the rejections.

Applicant has amended the independent claims to add a limitation comparable to claim 11 that the trace data order signal specifies a transfer of trace data for a particular instruction that is specified relative to at least one instruction for which there is outstanding trace data. As described in Applicant's specification on paragraphs [1036] to [1038], data associated with an instruction may not be immediately available to be traced out. Thus, in some cases the instruction is traced out before its associated trace data. This may result in a situation in which one or more instructions have been traced out but the associated trace data is outstanding. The trace data order signal provides information on the relative position of the trace data being traced out relative to other instructions having outstanding trace data.

As an illustrative example, consider the embodiment described in paragraph [1040]. Load data generated by a load instruction may in some cases not be available in a cache, resulting in a time delay between the instance of the load instruction and the return of load data from memory. As described in paragraph [1040], in one embodiment a trace data order determination element generates a signal that indicates the position of trace data relative to previously traced instructions for which trace data was delayed. For the case of load data, the load data, a trace data order signal may specify the position of load data with respect to the relative age of previous instructions that were traced out but for which the associated trace data was not immediately available (e.g., a load order with respect to a first oldest instruction, a second oldest instruction, a third oldest instruction, etc.).

One benefit of Applicant's claimed invention is that it facilitates tracing trace data as the trace data become available. As described in paragraph [1036], tracing trace data as it becomes available avoids the need to save trace data that hits in the cache while waiting for earlier trace data missed in the cache to return. The trace data order signal permits, for example, the correct association to be made between elements of trace data that were delayed by one or more cycles (e.g., a cache miss) to the instructions that generated them.

Applicant respectfully submits that the cited references do not teach or suggest the limitation of using a tracing data order signal to specify a trace data order relative to instructions having outstanding trace data. As the Examiner has stated in paragraph 2 of

the Office Action, Miura does not teach or suggest a trace data order that is different than the program sequence of instructions. Miura relies upon FIFO buffers to trace data exactly in its original sequence. Referring to Figure 3 of Miura, Miura is configured with FIFO buffers 32A and 32B for debug data received directly from an instruction execution unit (IEU). Miura teaches a system in which an instruction execution unit transmits branch source addresses from an instruction execution unit 31 to a branch instruction address FIFO buffer FJA 32A, as described in column 8, lines 20-25. The instruction execution unit also transmits memory data to a memory data FIFO buffer FRW 32B whenever memory data is accessed, as described in column 8, lines 27-32. The FIFO buffers are first in, first out buffers such that there is no trace order determination. Each entry in FIFOs 32A and 32B also include a counter count to indicate the sequence of the branch instruction and the memory access instruction executed and transmitted by the IEU 31, as described in column 8, lines 34-40.

Miyake discloses a processing apparatus having out-of-order execution of instructions. Miyake is directed to the problem of dealing with data dependencies in out-of-order execution, such as for example, detection of data dependency of execution instructions, as described in column 5, lines 3-12. However, Miyake does not teach or suggest a tracing apparatus of any kind.

Swaine discloses a tracing system for tracing data in a processor that may have a data access miss, as described in paragraph [0007] of Swaine. However, Swaine does not have a data order signal that specifies a transfer order relative to instructions having outstanding trace data. Instead, Swaine requires the transmission of a data place holder 32 that must be placed into a trace data stream exactly at a point corresponding to an instruction that generates a miss, as described in paragraph 45 of Swaine. When data becomes available for the instruction that generated the miss, a tag value is associated with the data value to permit it to be matched to the placeholder, as described in paragraph 45 of Swaine.

Independent claims 1, 8, and 10 were rejected under 35 U.S.C. §103 in light of Miyaka and Miura. However, Miyake and Miura do not have a trace data order determination element as required by independent claims 1, 8, and 10. Additionally, neither reference teaches or suggests a trace data order signal to specify a trace data order

relative to instructions having outstanding trace data. While Miyake can execute instructions in an order that is different from the instruction order, it has no provision for tracing data. Miura has no provision for coordinating trace data for out-of-order data. The FIFO's of Miura collects memory data in a first-in, first out manner which would not permit out-of-order trace data to be associated with its corresponding instruction. Consequently, Applicant respectfully submits that the references cannot be combined in the manner stated by the Examiner. In regards to Swaine, Applicant notes that Swaine teaches away from a trace data order that is relative to instructions having trace data outstanding since Swaine requires data holders to be inserted into the trace data stream and utilizes tags to match late data with its placeholder.

In regards to independent claims 11 and 20, the Examiner rejected these claims in light of Miura in view of Miyake and further in view of Swaine. The cited art does not teach or suggest a trace data order relative to instructions having trace data outstanding. As previously described, Swaine requires data holders to be inserted into the trace data stream and utilizes tags to match late data with the place holders. Consequently, Applicant respectfully submits that the cited references cannot be combined to achieve Applicant's claimed invention.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is now in condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No. 03-3117.

Dated: April 2, 2004

By:

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